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27. (Twice Amended) An integrated circuit, comprising:

semiconductor devices, including;

a semiconductor substrate;

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a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover;

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a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions; and

interconnect structures contacting the semiconductor devices.

(10) Kindly rewrite Claim 31 as follows:

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31. (Amended) The integrated circuit as recited in Claim 27 wherein the second portion comprises polysilicon.

REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the following remarks.

The Applicant originally submitted Claims 1-33 in the application. In a previous response to an Official Action, the Applicant canceled Claim 33 without prejudice or disclaimer. Presently,

the Applicant has amended Claims 1, 5, 7, 10, 12, 17, 21, 25, 27 and 31 and has neither canceled nor added any other claims. Accordingly, Claims 1-32 are currently pending in the application.

I. Rejection of Claims 1-4, 7-9, 12, 13, 16, 17, 18, and 21-24 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4, 7-9, 12, 13, 16, 17, 18, and 21-24 under 35 U.S.C. §102(b) as being clearly anticipated by U.S. Patent No. 5,391,907 to Jang (Jang). Presently, newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that the source/drain regions include first and second portions separated by an interface. Jang fails to disclose such an element. Because the source/drain region 20 of Jang is formed in the substrate 11 using a single step, it cannot have the interface required by the present invention. Accordingly, Jang fails to disclose the element that the source/drain regions include first and second portions separated by an interface.

Therefore, Jang does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-4, 8-9, 13, 16, 18, and 22-24 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Jang also cannot be an anticipating reference for Claims 2-4, 8-9, 13, 16, 18, and 22-24. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

II. Rejection of Claims 1-4, 7-9, 12-13, 16, 17-18, 21-24, 27-30 and 33 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4, 7-9, 12-13, 16, 17-18, 21-24, 27-30 and 33 under 35 U.S.C. §102(b) as being clearly anticipated by U.S. Patent No. 4,551,743 to Murakami (Murakami). As previously recited, newly amended independent Claims 1, 7, 12, 17, 21, and 27

include the element that the source/drain regions include first and second portions separated by an interface. Murakami fails to disclose such an element. Murakami does disclose that its source/drain regions 19, 20 are entirely diffused within its semiconductor substrate 10 in a single processing step, however, such a teaching inherently prevents the formation of the interface required by the present invention. Accordingly, Murakami fails to disclose the element that the source/drain regions include first and second portions separated by an interface.

Therefore, Murakami does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-4, 8-9, 12-13, 16, 18, 22-24, 28-30 and 33 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Murakami also cannot be an anticipating reference for Claims 2-4, 8-9, 12-13, 16, 18, 22-24, 28-30 and 33. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

III. Rejection of Claims 1-32 under 35 U.S.C. §102

The Examiner has rejected Claims 1-32 under 35 U.S.C. §102(b) as being clearly anticipated by Japanese Patent No. 11-274483A to Tsuchiaki (Tsuchiaki). Newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that the isolation region includes a first portion and a second post portion located thereover. Tsuchiaki fails to disclose such an element, among others.

Tsuchiaki is directed to a field-effect transistor having an elevated source/drain portion. (Abstract) Tsuchiaki teaches that shallow trench isolation structures 12 separate the n-type diffusion layer 22 and the p-type diffusion layer 25. Tsuchiaki does not teach, however, that its shallow trench

isolation structures 12 include a first portion and a second post portion located thereover. Accordingly, Tsuchiaki fails to disclose the element that the isolation regions include a first portion and a second post portion located thereover, as required by the independent claims of the present invention.

Therefore, Tsuchiaki does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-6, 8-11, 13-16, 18-20, 22-26, and 28-32 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Tsuchiaki also cannot be an anticipating reference for Claims 2-6, 8-11, 13-16, 18-20, 22-26, and 28-32. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

IV. Rejection of Claims 27-30 under 35 U.S.C. §103

The Examiner has rejected Claims 27-30 under 35 U.S.C. §103(a) as being obvious over Jang in view of the Applicant's admitted prior art (APA). As recited above, Jang fails to disclose every element recited in independent Claims 1, 7, 12, 17, 21 and 27. Namely, Jang fails to disclose the element that the source/drain regions include first and second portions separated by an interface.

Similarly, it is the position of the Applicant that Jang also fails to suggest the element that the source/drain regions include first and second portions separated by an interface. Jang fails to suggest such an element because Jang is focused on forming its source/drain regions in its semiconductor substrate using a single diffusion process. Given the structure illustrated and described in Jang, as well as the method taught to manufacture such a device, one skilled in the art would not be motivated to create an interface between a first portion of its source/drain regions and

a second portion of its sourc /drain region. Accordingly, Jang fails to teach or suggest such an element.

The Examiner is using the APA for the sole proposition that interconnects may be used to connect the claimed device to various other active and passive devices. Notwithstanding the merits of the Examiner's proposition, the APA also fails to teach or suggest the element that the source/drain regions include first and second portions separated by an interface. A teaching or suggestion of an interconnect connecting various devices is dissimilar to a teaching or suggestion that the source/drain regions include first and second portions separated by an interface.

Therefore, the combination of Jang and the APA fails to teach or suggest each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, it fails to establish a *prima facie* case of obviousness with respect to independent Claims 1, 7, 12, 17, 21 and 27, and any claims dependent therefrom.

In view of the foregoing amendments and remarks, the cited references do not support the Examiner's rejection of Claim 27-30 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

V. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-32.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.

Greg H. Parker
Registration No. 44,995

Dated: 7-19-02

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800

DOCKET NO. WYLIE 5

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

(1) Kindly rewrite Claim 1 as follows:

1. (Twice Amended) A semiconductor device, comprising:

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover;

[at least a portion of one of a source/drain region formed on the isolation region, but not in the semiconductor substrate] a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(2) Kindly rewrite Claim 5 as follows:

5. (Amended) The semiconductor device as recited in Claim 1 wherein [a portion of the at least one source/drain region] the second portion comprises polysilicon.

(3) Kindly rewrite Claim 7 as follows:

7. (Twice Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation region located in the trench, wherein the isolation region includes a first portion and a second post portion located thereover; and

[at least a portion of one of a source/drain region located on the isolation region, but not in the semiconductor substrate] a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(4) Kindly rewrite Claim 10 as follows:

10. (Amended) The semiconductor device as recited in Claim 7 wherein the [source/drain region includes a first portion located in the semiconductor substrate and a] second portion [comprising] comprises polysilicon [located on the isolation region].

(5) Kindly rewrite Claim 12 as follows:

12. (Twice Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

an isolation region located adjacent the channel region, the isolation region being located within a trench formed in the semiconductor substrate and not extending under the channel region and including a first portion and a second post portion located thereover; and

source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(6) Kindly rewrite Claim 17 as follows:

17. (Twice Amended) A semiconductor device, comprising:

a first transistor located adjacent a second transistor, wherein both the first and second transistors are located over a semiconductor substrate;

an isolation region located between the first and second transistors and within a trench located within the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover; and

source/drain regions associated with each of the first and second transistors, each of the source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(7) Kindly rewrite Claim 21 as follows:

21. (Twice Amended) A method of manufacturing a semiconductor device, comprising:

providing a semiconductor substrate;

creating a gate above the semiconductor substrate;

forming an isolation region within a trench located in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover;

[forming at least a portion of one of a source/drain region above the isolation region, but not in the semiconductor substrate] forming a first portion of one of a source/drain region in the semiconductor substrate and a second portion of the one of the source/drain region on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(8) Kindly rewrite Claim 25 as follows:

25. (Amended) The method as recited in Claim 21 wherein forming [the at least one source/drain region includes forming a portion of the at least source/drain region] a second portion includes forming a second portion with polysilicon.

(9) Kindly rewrite Claim 27 as follows:

27. (Twice Amended) An integrated circuit, comprising:

semiconductor devices, including;

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover;

[at least a portion of one of a source/drain region formed above the isolation region, but not in the semiconductor substrate] a first portion of one of a source/drain region formed in the

semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions; and

interconnect structures contacting the semiconductor devices.

(10) Kindly rewrite Claim 31 as follows:

31. (Amended) The integrated circuit as recited in Claim 27 wherein [a portion of the at least one source/drain region] the second portion comprises polysilicon.